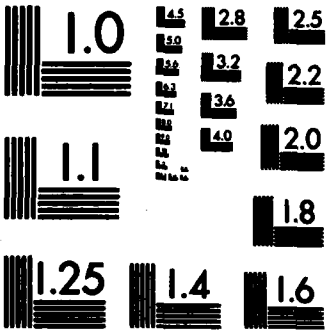
AD-A148 121 NUMERICAL ALGORITHMS AND PARALLEL TASKING(U) 1/1
MASSACHUSETTS INST OF TECH CAMBRIDGE LAB FOR
INFORMATION AND DECISION SYSTEMS V C KLEMA ET AL.
UNCLASSIFIED 14 MAY 83 AFOSR-TR-83-0978 AFOSR-82-0210 F/G 12/1 NL



REPORT DOCUMENTATION PAGE

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1. REPORT NUMBER: AFOSR-TR-83-0978	2. GOVT ACCESSION NO.
3. RECIPIENT'S CATALOG NUMBER	
4. TITLE (and Subtitle): NUMERICAL ALGORITHMS AND PARALLEL TASKING	5. TYPE OF REPORT & PERIOD COVERED: INTERIM, 15 MAY 82-14 MAY 83
6. PERFORMING ORG. REPORT NUMBER	
7. AUTHOR(s): Virginia C. Klema and Elizabeth R. Ducot	8. CONTRACT OR GRANT NUMBER(s): AFOSR-82-0210
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Laboratory for Information & Decision Systems, Massachusetts Institute of Technology, Cambridge MA 02139	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: PE61102F; 2304/A3
11. CONTROLLING OFFICE NAME AND ADDRESS: Mathematical & Information Sciences Directorate, Air Force Office of Scientific Research/NM, Bolling AFB DC 20332	12. REPORT DATE: 14 MAY 83
	13. NUMBER OF PAGES: 3
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)	15. SECURITY CLASS. (of this report): UNCLASSIFIED
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

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17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

During this period the hardware configuration of four Intel 8630 boards each having an Intel 8086 central processing unit and an 8087 numeric data processor with IEEE floating point arithmetic has been installed and is operational. Fortran 77 (the subset with certain extensions to support IEEE floating point arithmetic) is operational for numerical computing. ASM86 (the Intel assembly language) and PLM (the Intel systems programming language) are used for the necessary operating systems work to permit concurrent computing on the Intel processors.

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AFOSR-TR- 83-0978

Progress Report, AFOSR ~~reference number~~ 82-0210, contract #2304/A3, "Numerical Algorithms and Parallel Tasking," principal investigator, Virginia C. Klema, research staff member, Elizabeth R. Ducot.

During the period, May 15, 1982 through May 14, 1983, Virginia Klema and Elizabeth Ducot have been supported for four months. During this period of time the hardware configuration of four Intel 8630 boards each having an Intel 8086 central processing unit and an 8087 numeric data processor with IEEE floating point arithmetic has been installed and is operational. Fortran 77 (the subset with certain extensions to support IEEE floating point arithmetic) is operational for numerical computing. ASM86 (the Intel assembly language) and PLM (the Intel systems programming language) are used for the necessary operating systems work to permit concurrent computing on the Intel processors.

The concurrent computing system is augmented by the Intel 432 32 bit processors (four at present). These processors were donated by the Intel Corporation for this research. The Intel 432 system receives native code by cross-compilation of Ada (trademark of DoD) files that are compiled, linked, and downloaded to the Intel development system (provided by National Science Foundation resources) that serves as a front end machine for the 432 system. The post-doctoral associate, A. R. Barron has done most of the work on Ada thus far.

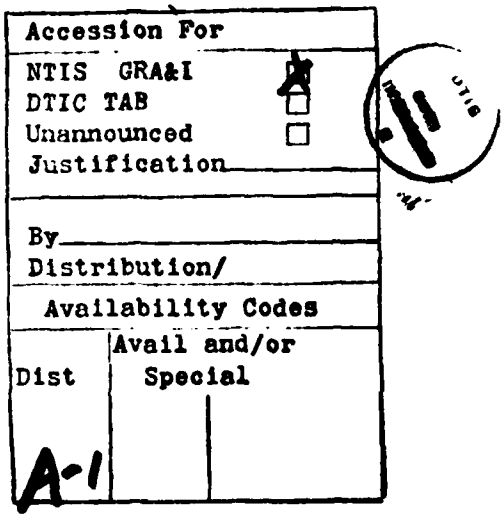
The hardware configuration will be augmented by additional Intel processors and a VAX 11/730 dedicated to this research. These components are provided by the DoD Instrumentation grant to Virginia Klema administered by AFOSR.

Results of the research will be reported in an invited address by Virginia Klema at the Toronto American Statistical Association in August. Elizabeth Ducot and Virginia Klema will present a summary of the Computing environment for concurrent computing at the SIAM Conference on Parallel Computing in Norfolk in November. Copies of these presentations will be submitted to AFOSR.

We enclose Elizabeth Ducot's comments on the progress of the work on the parallel tasker for which she has primary responsibility.

We gratefully acknowledge the support for this research.

Virginia Klema
June 14, 1983



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PROGRESS REPORT

The hardware for the Experimental Concurrent Computing Testbed (preliminary version) has been installed at MIT. The initial configuration is an example of a global bus architecture in which intel 8086/8087 processor/co-processor pairs are connected via a common multibus. (Upgrades of the main procesor to the more powerful 286 (386) processor chips can be accommodated in the system as configured; constraints on the upgrade will be due to the availability of the companion 287 (387) numeric data processors).

The design of the computing environment for this multi-processor system calls for one of the 8086 processors to function as the system MANAGER (MP). The manager has the highest priority in the system and is responsible for most of the system functions (including file manipulation, system I/O, and interaction with the user). In addition, the system manager will host the parallel tasker and will act as a controller for the execution of the parallel algorithms. Depending on the algorithm, portions of the computation may be performed by the manager; hence a numeric data processor (intel 8087) has been included as a part of the MP processing element. Subordinate to the MP are WORKER processing elements (WP's), consisting of identical 8086/8087 pairs. Currently, there are three WP's in place within the system; additional components are expected in the fall of 1983.

Mechanisms have been established that provide for communication among processors, for interprocessor coordination, and for conflict resolution. Communication will be achieved via uni-directional software ports located in shared memory. In order to minimize bus contention inherent in a fully shared memory scheme, the ports and associated buffers are placed in regions that, while <u>logically</u> accessible to all elements on the multibus, are <u>physically</u> on-board the receiving processor. In this implementation, the receiver is viewed as the "owner" of the port region, using only its local data bus to access code and data and status information located there. Parallel priority logic, implemented in hardware, is used to resolve contention on the multibus. Port contention and mutual exclusion logic will be implemented in software. The development of code for creating the ports and establishing the specialized communication primitives is in progress, and the testing of the mechanisms for shifting code modules from the MP to a WP is underway. Semantics for specifying the algorithmic decomposition and process coordination logic, based on these primitives, are in the early design stages.

Elizabeth R. Ducot
June 14, 1983

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